Amendment to the Specification:

Please replace the paragraph on p. 12, lines 16 to 23 with the following amended paragraph:

A gate terminal 312 of a second FET M2 is coupled to the node PD. A drain terminal 314 of the FET M2 is coupled to the supply voltage Vdd and a source terminal 316of the FET M2 is coupled to a drain terminal 318 of a third FET M3. A gate terminal 320 of the FET M3 is coupled to the row line 130. A source terminal ~~322of~~ 322 of the FET M3 is coupled to the column line 150. The FETs M2 and M3 comprise n-channel enhancement mode MOSFETs.

Please replace the paragraph on p. 14, line 24 to p. 15, line 9 with the following amended paragraph:

The sample reset interval begins at time T2 with the row reset circuit 104 (FIGs. 1 and 2) supplying the ground referenced reset voltage to the gate terminal 306 of the reset FET M1, causing the reset FET M1 to turn on. With the reset FET M1 on, the voltage at node PD increases to the ground referenced reset voltage at time T3 minus the threshold voltage of the reset FET M1. The sample reset interval extends from time T2 to time T3 and may have a duration substantially equal to that of the exposure reset time. [[at]] At time T3, the reset voltage is pulled to ground.